REMARKS

This Amendment/Reply accompanies the Request for Continued Examination (RCE) 37 CFR 1.114 and is in reply to the Final Office Action mailed November 1, 2007.

The following remarks are made in response to the Final Office Action mailed November 1, 2007. Claim 38 has been cancelled. Claims 22-25 and 27-43 were rejected. With this Response, claims 22, 41 and 44 have been amended and claims 44-45 added. Claims 22-25, 27-37 and 39-45 remain pending in the application and are presented for reconsideration and allowance.

In the Drawings

The Examiner has objected to the drawings under 37 C.F.R. 1.83(a) reciting that the drawings must show every feature of the invention specified in the claims. Applicants have cancelled claim 38, which was the only claim reciting the feature referred to by the Examiner. As such, cancellation of claim 38 overcame the objection to the drawings. Applicants believe the drawings are now in condition for allowance.

In the Specification

The Examiner has objected to the title because it is not descriptive. Applicants have amended the title. Applicants believe the title is now in condition for allowance.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 22-25, 27-28, and 30-43 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Publication No. 2001/0023986 in view of the Choi et al. U.S. Publication No. 2002/0001905. Also, the Examiner rejected claim 29 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Publication No. 2001/0023986 in view of the Martin et al. U.S. Publication No. 2001/0019279.

Claim 22 as amended is a vertically integrated field-effect transistor including a first electrically conductive layer, a middle layer formed partially from dielectric material on the first

electrically conductive layer, a second electrically conductive layer on the middle layer, and a nanostructure integrated in a via hole introduced into the middle layer. The nanostructure further includes a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer. The first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor. ***The middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer***, the thickness of which is less than the thickness of at least one of the dielectric sublayers. ***A ring structure*** is formed from an electrically insulating material as gate-insulating region of the field-effect transistor ***is formed from and arranged in*** the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein. Support for the amendment is at least on page 5, paragraph [0055], lines 9 to 17 of the specification of the published application (US 2006/0128088 A1).

The *Mancevski* reference fails to teach or suggest that a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is formed from and arranged in a third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein. In fact, the *Mancevski* reference neither discloses nor suggests providing any gate-insulating region at all.

Furthermore, the *Choi* reference discloses a vertical field-effect transistor (Fig. 1) having a vertically grown carbon nanotube 100 as a channel arranged in a hole 10', which is filled with a non-conductor film 30. A gate 20 that is electrically insulated from the nanotube 100 by the non-conductor film 30 serves to control current flow in the nanotube (channel) 100 between source and drain regions 40, 50 of the transistor. The non-conductor film 30 is formed by deposition of material onto the gate 20, thereby filling the hole 10'.

The *Choi* reference fails to cure the deficiencies of he *Mancevski* reference, in that *Choi* neither discloses nor suggests that an insulating ring structure is formed from and arranged in a third electrically conductive layer, which forms the gate electrode of the field-effect transistor. The *Choi* reference discloses that a nonconductor film 30 is deposited over the gate 20 to fill

the hole 10' (e.g. paragraphs [0028] and [0036] in *Choi*). That is, the nonconductor film 30 is not formed from material of the gate 20 but by deposition of a separate layer onto the gate 20 and onto the hole 10', thereby filling the entire hole 10' with material of the nonconductor film.

In contrast thereto, in the vertically integrated field-effect transistor in accordance with amended claim 22, the ring structure is formed from the material of a third electrically conductive layer that is arranged between two adjacent dielectric sublayers. As such, the ring structure is formed from and arranged in the third electrically conductive layer along the via hole such that portions of the via hole above and below the ring structure remain free from material of the ring structure.

In the *Choi* reference, a non-conductor film 30 is formed by deposition of a layer over the gate 20 and the carbon nanotube 100, thereby filling the hole 10' and electrically insulating the carbon nanotube 100 from the gate 20. Thus, although the *Mancevski* reference does not suggest to provide a gate-insulating region of any shape, even in case that a person of ordinary skill faced the task to provide a gate-insulating region in the transistor structure of the *Mancevski* reference, he would merely learn to deposit a non-conductor film over the holes disclosed inthe *Mancevski* reference such that the holes are filled with the non-conductor film. Thus, the person of ordinary skill would end up with a structure different from the subject-matter of claim 22, as amended.

The subject matter of claims 41 and 43, as amended are similar to amended claim 22, and thus, are believed to be non-obvious over *Mancevski* in view of *Choi* for at least the reasons given above. Claims 23-25, 27-37, 39-40 and 42 are ultimately dependent on one of claims 22 and 41 and recite further limitations. Thus, they are believed to be non-obvious over *Mancevski* in view of *Choi* for at least the same reasons.

Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection to claims 22-25, 27-37 and 39-43, and request allowance of these claims.

Added Claims 44 and 45

With regard to new claims 44 and 45 are in condition for allowance for similar reasons. New claim 44 provides a vertically integrated field-effect transistor, including a middle layer, formed partially from dielectric material, on the first electrically conductive layer. The middle layer has ***an additional electrically conductive layer, which at least one additional electrically conductive layer serves as an additional gate electrode of the field-effect transistor, with an additional ring structure formed from an electrically insulating material as an additional gate-insulating region of the field-effect transistor being arranged along the via hole that has been introduced in the additional electrically conductive layer.***"

None of the cited references disclose or suggest a vertically integrated field-effect transistor, wherein a middle layer has an additional electrically conductive layer, which at least one additional electrically conductive layer serves as an additional gate electrode of the field-effect transistor, with an additional ring structure formed from an electrically insulating material as an additional gate-insulating region of the field-effect transistor being arranged along the via hole that has been introduced in the additional electrically conductive layer.

The Examiner argues that it would have been obvious to one of ordinary skill to add an additional electrically conductive layer and ring structure in the structure of *Mancevski*, since it has been held that mere duplication of the essential working parts of a device involve only routine skill in the art.

However, the *Mancevski* reference neither discloses nor suggests that a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in a third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein. In fact, the *Mancevski* reference neither discloses nor suggests to provide any gate-insulating region at all, as described above.

Furthermore, provision of an additional electrically conductive layer as additional gate electrode with an additional ring structure as additional gate-insulating region cannot be considered as a mere duplication of the essential working parts. One effect of the additional gate

electrode is, for example, that a further improvement of the controllability of the electrical resistance of the nanostructure may be achieved. Clearly, by means of the (at least one) additional gate electrode, the electrical conductivity of the nanostructure may be influenced independently at different subregions of the nanostructure or, alternatively, may be influenced at a plurality of subregions simultaneously, which leads to an improved controllability of the electrical resistance of the nanostructure.

The *Mancevski* reference neither discloses nor suggests an additional gate electrode or ring structure or the above-described effects. The subject-matter of new claim 44 is thus believed to be non-obvious over the *Mancevski* reference for at least the reasons given above. The same holds true for new method claim 45, which recites similar limitations.

Therefore, Applicants respectfully request allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 22-25 and 27-43 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 22-25 and 27-43 are respectfully requested.

Applicants hereby authorize the Commissioner for Patents to charge Deposit Account No. 50-0471 in the amount of $420.00 to cover the fees as set forth under 37 C.F.R. 1.16(h)(i).

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Paul P. Kempf at Telephone No. (612) 767-2502, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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